IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Yosef Solt et al.	Art Unit	: 2189
Serial No.	: 10/809,537	Examiner	: Bragdon, Reginald Glenwood
Filed	: March 24, 2004	Conf. No.	: 6150
Title	: BUFFER MANAGEMENT ARCHITECTURE		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Applicants file this brief on appeal under 37 CFR § 41.37, in response to the Notice of Panel Decision from Pre-Appeal Brief Review mailed on April 11, 2008 and to the Notification of Non-Complaint Appeal Brief mailed on May 21, 2008.

The sections required by 37 CFR § 41.37 follow.

(1) Real Party in Interest

Marvell Semiconductor Israel Ltd., the assignee of this patent application, is the real party in interest.

(2) Related Appeals and Interferences

There are no related appeals or interferences.

(3) Status of Claims

Currently, claims 1-111 are pending in the action of which claims 9-17, 27-36, 46-55, 65-74, 84-93 and 102-110 have been withdrawn. Claims 1, 18, 37, 56, 75 and 94 are independent, and claims 7-8, 24-25, 62-63, 81-82 and 100-101 have been indicated to contain allowable subject matter. Applicants appeal the rejection of claims 1-8, 18-26, 37-45, 56-64, 75-83, 94-101 and 111.

(4) Status of Amendments

The claims have not been amended subsequent to the final office action mailed November 1, 2007, and there are no unentered amendments.

(5) Summary of Claimed Subject Matter

Claim 1

Claim Language	Support in Specification and/or FIGS.
A method comprising:	*See e.g.,* Fig. 3.
writing one of a plurality of sets in an allocation memory into an allocation register,	*See e.g.,* ¶ [0015], lines 1-3; and allocation SRAM 202 and allocation register 204 in Fig. 2.
wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;	*See e.g.,* ¶ [0014], lines 3-5; and buffer memory 106 in Fig. 1.
in response to an allocation request,	*See e.g.,* ¶ [0015], lines 1-6.
identifying a data element in the allocation register having a value corresponding to an available buffer;	*See e.g.,* ¶ [0014], lines 12-15; ¶ [0015], lines 4-7; ¶ [0019], lines 6-8; and ¶ [0021], lines 1-4.
changing the value of said data element to a value corresponding to an allocated buffer; and	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0021], lines 10-15.
allocating the buffer associated with said data element.	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0019], lines 10-12.

Claim 18

Claim Language	Support in Specification and/or FIGS.
An apparatus comprising:	*See e.g.,* Fig. 3.
an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;	*See e.g.,* ¶ [0014], lines 3-5; and allocation SRAM 202 in Fig. 2 and buffer memory 106 in Fig. 1.
an allocation register; and	*See e.g.,* allocation register 204 in Fig. 2.
a buffer manager to write one of said plurality of sets into the allocation register, and	*See e.g.,* buffer management 108 in Fig. 1.
in response to an allocation request,	*See e.g.,* ¶ [0015], lines 1-6.
identify a data element in the allocation register having a value corresponding to an available buffer,	*See e.g.,* ¶ [0014], lines 12-15; ¶ [0015], lines 4-7; ¶ [0019], lines 6-8; and ¶ [0021], lines 1-4.
change the value of said data element to a	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0021],

value corresponding to an allocated buffer and	lines 10-15.
allocate the buffer associated with said data element.	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0019], lines 10-12.

Claim 37

Claim Language	Support in Specification and/or FIGS.
An apparatus comprising:	*See e.g.,* Fig. 3.
an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;	*See e.g.,* ¶ [0014], lines 3-5; and allocation SRAM 202 in Fig. 2 and buffer memory 106 in Fig. 1.
an allocation register; and	*See e.g.,* allocation register 204 in Fig. 2.
a buffer manager including	*See e.g.,* buffer management 108 in Fig. 1.
means for writing one of said plurality of sets into the allocation register, and	*See e.g.,* ¶ [0004], lines 26-29.
means for, in response to an allocation request,	*See e.g.,* ¶ [0015], lines 1-6.
identifying a data element in the allocation register having a value corresponding to an, available buffer,	*See e.g.,* ¶ [0014], lines 12-15; ¶ [0015], lines 4-7; ¶ [0019], lines 6-8; and ¶ [0021], lines 1-4.
changing the value of said data element to a value corresponding to an allocated buffer, and	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0021], lines 10-15.
allocating the buffer associated with said data element.	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0019], lines 10-12.

Claim 56

Claim Language	Support in Specification and/or FIGS.
A system comprising:	*See e.g.,* Fig. 1.
a switching module to receive and switch packets;	*See e.g.,* switch 100 in Fig. 1.
a buffer memory including a plurality of buffers to store received packets; and	*See e.g.,* ¶ [0012], lines 5-7; and buffer memory 106 in Fig. 1.
a buffer management module including:	*See e.g.,* buffer management 108 in Fig. 1.
an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding one of the	*See e.g.,* ¶ [0014], lines 3-5; and allocation SRAM 202 in Fig. 2 and buffer memory 106 in Fig. 1.

plurality of buffers in the buffer memory;	
an allocation register; and	*See e.g.,* allocation register 204 in Fig. 2.
a buffer manager to write one of said plurality of sets into the allocation register, and	*See e.g., .,* ¶ [0004], lines 26-29; and buffer management 108 in Fig. 1.
in response to an allocation request,	*See e.g.,* ¶ [0015], lines 1-6.
identify a data element in the allocation register having a value corresponding to an available buffer,	*See e.g.,* ¶ [0014], lines 12-15; ¶ [0015], lines 4-7; ¶ [0019], lines 6-8; and ¶ [0021], lines 1-4.
change the value of said data element to a value corresponding to an allocated buffer, and	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0021], lines 10-15.
allocate the buffer associated with said data element.	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0019], lines 10-12.

Claim 75

Claim Language	Support in Specification and/or FIGS.
A system comprising:	*See e.g.,* Fig. 1.
a switching module including means for receiving and switching packets;	*See e.g.,* switch 100 and ports 102 in Fig. 1.
a buffer memory including a plurality of buffers for storing received packets; and	*See e.g.,* ¶ [0012], lines 5-7; and buffer memory 106 in Fig. 1.
a buffer management module including:	*See e.g.,* buffer management 108 in Fig. 1.
an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;	*See e.g.,* ¶ [0014], lines 3-5; and allocation SRAM 202 in Fig. 2 and buffer memory 106 in Fig. 1.
an allocation register; and	*See e.g.,* allocation register 204 in Fig. 2.
a buffer manager including	*See e.g.,* buffer management 108 in Fig. 1.
means for writing one of said plurality of sets into the allocation register, and	*See e.g.,* ¶ [0004], lines 26-29.
means for, in response to an allocation request,	*See e.g.,* ¶ [0015], lines 1-6.
identifying a data element in the allocation register having a value corresponding to an available buffer,	*See e.g.,* ¶ [0014], lines 12-15; ¶ [0015], lines 4-7; ¶ [0019], lines 6-8; and ¶ [0021], lines 1-4.
changing the value of said data element to a value corresponding to an allocated buffer, and	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0021], lines 10-15.
allocating the buffer associated with said data element.	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0019], lines 10-12.

Claim 94

Claim Language	Support in Specification and/or FIGS.
A computer-readable medium having instructions stored thereon, which, when executed by a processor, causes the processor to perform operations comprising:	*See e.g.,* ¶ [0011], lines 1-5.
writing one of a plurality of sets in an allocation memory into an allocation register,	*See e.g.,* ¶ [0015], lines 1-3; and allocation SRAM 202 and allocation register 204 in Fig. 2.
wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;	*See e.g.,* ¶ [0014], lines 3-5; and buffer memory 106 in Fig. 1.
in response to an allocation request,	*See e.g.,* ¶ [0015], lines 1-6.
identifying a data element in the allocation register having a value corresponding to an available buffer;	*See e.g.,* ¶ [0014], lines 12-15; ¶ [0015], lines 4-7; ¶ [0019], lines 6-8; and ¶ [0021], lines 1-4.
changing the value of said data element to a value corresponding to an allocated buffer; and	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0021], lines 10-15.
allocating the buffer associated with said data element.	*See e.g.,* ¶ [0015], lines 6-7; and ¶ [0019], lines 10-12.

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 1-6, 18-23, 26, 37-42, 45, 56-61, 64, 75-80, 83, 94-99 and 111 are rejected as allegedly being anticipated by USP No. RE 38,821 to **Shemla**. Applicants respectfully request that these rejected claims be reviewed on appeal.

(7) Argument

Section 102(e) Rejections

Claims 1-6, 18-23, 26, 37-42, 45, 56-61, 64, 75-80, 83, 94-99 and 111 are rejected as allegedly being unpatentable over **Shemla**. Applicants respectfully traverse this rejection.

A. Shemla's Hash Table Are Not Sets

Claim 1 recites in part writing **one of a plurality of sets** in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets.

In the Office Action dated February 6, 2007 ("Office Action"), the Examiner asserted that Shemla's hash table 212 corresponds to the claimed allocation memory, and Shemla's hash table locations correspond to the claimed sets. *See*, page 4, lines 11-12 of Office Action.

In the Response filed August 21, 2007 ("Response"), Applicants argued, *inter alia*, that Shemla's hash table 212 does not include "a plurality of sets" because each of Shemla's hash table locations is not an individual set or one that is included in one of a plurality of sets collectively. *See*, page 30, last 2 lines of the Response.

In the Final Office Action dated November 1, 2007 ("Final Office Action"), the Examiner maintained that Shemla's hash table locations are "sets", citing elements 212, 222, 224, 225 and 220 as support. *See*, page 6, lines 16-18 of Final Office Action.

Applicants respectfully submit that Shemla's hash table locations are not sets. Rather, Shemla's hash table locations are source and destination addresses that have been transformed into table locations via hash functions (8:39-42). As described in Shemla, each hash table location stores its own associated address information (8:45-53). This allows Shemla to identify which locations are empty and which empty locations in the table are "next" for an incoming packet without using pointers (8:67-9:3). In one example, Shemla provides that a packet can jump from table location 6 to location 11 and to location 16 (or until which there's a match between the input address and the address associated with a location) (8:54-64). Shemla's hash table locations are not sets, but are address locations that indicate where a packet is to be transmitted. *See also* col. 9, lines 37-41. For at least this reason, claim 1 is allowable over the relied upon portions of Shemla.

B. Shemla Does Not Write The Alleged Sets In An Allocation Memory Into An Allocation Register

Further, Applicants respectfully submit that claim 1 also recites **writing one of a plurality of sets in an allocation memory into an allocation register**. The Examiner indicates

that Shemla's request register 64 is the claimed allocation register, thus suggesting that Shemla writes the hash table locations into the request register 64. *See* page 3, lines 10-11 of Final Office Action.

Applicants respectfully submit that even assuming for the sake of argument (a point Applicants do not concede) that Shemla's hash table locations are sets, Shemla writes only buffer request messages into the request register 64. The relied upon portions of Shemla do not teach or suggest writing anything other than buffer request messages into the request register 64. As explicitly described in Shemla, the transfer manager 62, which is responsible for transferring a pending packet in the queue, writes a buffer request message into the request register 64 prior to transferring the packet (5:37-43), which causes the empty list block 50 to allocate an available buffer in the DRAM 20 for the packet (5:44-47). The relied on portions of Shemla do not teach or suggest writing the hash table locations (or associated address information) into the request register 64.

C. Shemla Does Not Identify A Data Element In An Allocation Register Or Changing The Value Of The Data Element

Further, claim 1 recites in part **identifying a data element** in an allocation register having a value corresponding to an available buffer, and **changing the value** of the data element to a value corresponding to an allocated buffer.

In the previous Response, Applicants argued that Shemla does not identify a data element in the buffer request message. Rather, Shemla's single-bit data element, whose value can be changed based on the empty or full state of an associated buffer, resides in the empty list block 50 of the switching unit 34 (2:21-31; 6:37-45), not in the request transfer register 64.

In the Final Office Action, the Examiner maintained that Shemla teaches these features at col. 10, lines 15-22 and col. 5, line 61-col. 6, line 9. *See*, page 7, lines 1-2 of Final Office Action. Specifically, by indicating that Shemla's request register 64 is the claimed allocation register, the Examiner is suggesting that Shemla identifies a data element in the request register 64, and changes the value of this data element to a value corresponding to an allocated buffer.

Applicants respectfully reiterate that Shemla identifies an empty buffer and changes its value in the empty list block 50, not in the request register 64. Shemla's section at col. 10, lines

15-22, as discussed above, is directed to writing a buffer request message to the request register 64. This paragraph provides no teaching or suggest of identifying a data element in the request register 64. The very fact that Shemla's empty list block 50 allocates an empty buffer 124 in the empty list 110 by changing the value of the empty buffer 124 (e.g., from "0" to indicate a buffer that is free to be written, to "1" to indicate a buffer that already stores a packet) (6:37-45) further evidences that Shemla: (1) identifies an available buffer in the empty list block 50, not in the request register 64; and (2) changes the buffer value of the available buffer in the empty list block 50, not in the request register 64. The relied upon portions of Shemla simply do not teach or suggest identifying a data element in an allocation register having a value corresponding to an available buffer, and changing the value of the data element to a value corresponding to an allocated buffer, as recited in claim 1.

Applicants respectfully submit that reading Shemla's empty list block 50 as an allocation register also would not cure the deficiencies in Shemla. In such a scenario, Shemla also would fail to write one of a plurality of sets, for Shemla has provided no mechanism for writing the hash table locations into the empty list block 50.

For at least the foregoing reasons, Applicants respectfully submit that Shemla does not anticipate claim 1. Claims 2-6 and 111 depend from claim 1, and also are submitted to be allowable for at least the same reasons set forth above with respect to claim 1.

Claim 18

Claim 18 recites in part a buffer manager to **write one of a plurality of sets** into an allocation register, **identify a data element** in the allocation register, and **change the value of the data element**.

As discussed above, the relied upon portions of Shemla do not teach or suggest these features. For at least the reasons similar to those discussed with respect to claim 1, Applicants respectfully submit that Shemla also does not anticipate claim 18. Claims 19-23 and 26 depend from claim 18, and also are submitted to be allowable for at least the same reasons set forth above with respect to claim 18.

Claim 37

Claim 37 recites in part an allocation memory including a plurality of data elements arranged in **a plurality of sets**, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory, a buffer manager including means for **identifying a data element** in the allocation register and means for **changing the value of the data element**.

As discussed above, the relied upon portions of Shemla do not teach or suggest these features. For at least the reasons similar to those discussed with respect to claim 1, Applicants respectfully submit that Shemla also does not anticipate claim 37. Claims 38-42 and 45 depend from claim 37, and also are submitted to be allowable for at least the same reasons set forth above with respect to claim 37.

Claim 56

Claim 56 recites in part a buffer manager to **write one of a plurality of sets** into an allocation register, **identify a data element** in the allocation register, and **change the value of the data element**.

As discussed above, the relied upon portions of Shemla do not teach or suggest these features. For at least the reasons similar to those discussed with respect to claim 1, Applicants respectfully submit that Shemla also does not anticipate claim 56. Claims 57-61 and 64 depend from claim 56, and also are submitted to be allowable for at least the same reasons set forth above with respect to claim 56.

Claim 75

Claim 75 recites in part a buffer manager including means for **writing one of a plurality of sets** into an allocation register, **identifying a data element** in the allocation register, and **changing the value of the data element**.

As discussed above, the relied upon portions of Shemla do not teach or suggest these features. For at least the reasons similar to those discussed with respect to claim 75, Applicants respectfully submit that Shemla also does not anticipate claim 75. Claims 76-80 and 83 depend from claim 75, and also are submitted to be allowable for at least the same reasons set forth above with respect to claim 75.

Claim 94

Claim 94 recites in part **writing one of a plurality of sets** into an allocation register, **identifying a data element** in the allocation register, and **changing the value of the data element**.

As discussed above, the relied upon portions of Shemla do not teach or suggest these features. For at least the reasons similar to those discussed with respect to claim 94, Applicants respectfully submit that Shemla also does not anticipate claim 94. Claims 95-99 depend from claim 94, and also are submitted to be allowable for at least the same reasons set forth above with respect to claim 94.

No fee is believed to be due. If necessary to keep the appeal brief active and pending, please apply any charges to Deposit Account No. 06-1050.

Respectfully submitted,

Date: June 18, 2008

/Alex Chan/
Alex Chan
Reg. No. 52,713

Customer No. 26200
Fish & Richardson P.C.
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

Appendix of Claims

1. A method comprising:

writing one of a plurality of sets in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

in response to an allocation request,

identifying a data element in the allocation register having a value corresponding to an available buffer;

changing the value of said data element to a value corresponding to an allocated buffer; and

allocating the buffer associated with said data element.

2. The method of claim 1, wherein each of the plurality of data elements comprises a single bit.

3. The method of claim 1, wherein each of the plurality of sets comprises a line in the allocation memory.

4. The method of claim 1, further comprising:

in response to a clear request for one of the plurality of buffers,

identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and

changing a value of said data element to the value corresponding to an available buffer.

5. The method of claim 4, further comprising:

in response to identifying the data element associated with said buffer in the allocation memory,

writing the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

writing the set in the clear register to the allocation memory.

6. The method of claim 1, further comprising:

monitoring the values of each of the data elements in the allocation register; and

in response to each of said data elements having the value corresponding to an allocated buffer,

writing the data elements in the allocation register back to the allocation memory;

identifying a set including at least one data element having the value corresponding to an available buffer; and

writing said set to the allocation register.

7. The method of claim 6, further comprising:

providing a vector including a plurality of data elements, ,each data element being associated with a corresponding one of the plurality of sets;

changing a value of a data element in the vector from the allocation register to a value corresponding to a full set in response to writing the set associated with said data element in the vector to the allocation memory; and

changing the value of said data element in the vector to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

8. The method of claim 7, further comprising:

identifying a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

9. A method comprising:

searching an allocation memory including a plurality of allocation data elements arranged in a second plurality of sets, each of said allocation data elements corresponding to an associated reclaim data element and the buffer associated with said reclaim data element;

searching a reclaim memory including a plurality of reclaim data elements arranged in a first plurality of sets, a plurality of said reclaim data elements being associated with a corresponding plurality of buffers in a buffer memory;

identifying one or more reclaim data elements to reclaim;

setting the value of said one or more reclaim data elements to reclaim data elements to a value corresponding to an available buffer; and

in a subsequent search, searching an allocation memory including a plurality of allocation data elements arranged in a second plurality of sets, each of said allocation data elements corresponding to an associated reclaim data element and the buffer associated with said reclaim data element;

comparing the allocation data elements to the associated reclaim data elements; and

changing the value of an allocation data element with a value corresponding to an allocated buffer to the value corresponding to an: available buffer in response to the associated reclaim data element having the value corresponding to an available buffer.

10. The method of claim 9, further comprising:

allocating the buffer associated with said allocation data element.

11. The method of claim 91, wherein each of the plurality of allocation data elements comprises a single bit, and

wherein each of the plurality of reclaim data elements comprises a single bit.

12. The method of claim 9, wherein the first plurality of sets comprises a plurality of lines in the allocation memory, and

wherein the second plurality of sets comprises a plurality of lines in the reclaim memory.

13. The method of claim 9, further comprising:

in response to receiving a trigger signal,

identifying each allocation data element, having the value corresponding to an allocated buffer; and

setting the value of each reclaim data element associated with said each allocation data element to the value corresponding to an allocated buffer.

14. The method of claim 9, further comprising:

reading one of said plurality of sets into an allocation register; and

allocating buffers based on the values of allocation data elements in the allocation;

register.

15. The method of claim 14, further comprising:

in response to a request to clear a buffer,

identifying an allocation data element associated with the buffer; and

in response to identifying said allocation data element in the allocation register, setting a value of said allocation element to the value corresponding to an available buffer; and

in response to not identifying said allocation data element in the allocation register,

writing the set including the allocation data element to an allocation clear register and setting a value of said

16. The method of claim 9, further comprising:

monitoring the values of the allocation data elements in the allocation register; and

in response to each of the allocation data elements in the allocation register having the value associated with an allocated buffer, writing the values of the set of allocation data elements to the allocation memory and to the reclaim memory.

17. The method of claim 9, wherein said identifying comprises identifying the one or more reclaim data elements to reclaim based on an aging time period.

18. An apparatus comprising:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

an allocation register; and

a buffer manager to

write one of said plurality of sets into the allocation register, and

in response to an allocation request,

identify a data element in the allocation register having a value corresponding, to an available buffer,

change the value of said data element to a value corresponding to an allocated

buffer, and

allocate the buffer associated with said data element.

19. The apparatus of claim 18, wherein each of the plurality of data elements comprises a single bit.

20. The apparatus of claim 18, wherein each of the plurality of sets comprises a line in the allocation memory.

21. The apparatus of claim 18, wherein the buffer manager is further operative to:

in response to a clear request for one of the plurality of buffers,

identify a data element associated with said buffer in one of the allocation memory and the allocation register; and

change a value of said data element to the value corresponding to an available buffer.

22. The apparatus of claim 21, wherein the buffer manager is further operative to:

in response to identifying the data element associated with said buffer in the allocation memory,

write the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

write the set in the clear register to the allocation memory.

23. The apparatus of claim 18, wherein the buffer manager is further operative to:

monitor the values of each of the data elements in the allocation register; and

in response to each of said data elements having the value corresponding to an allocated buffer,

write the data elements in the allocation register back to the allocation memory;

identify a set including at least one data element having the value corresponding to an available buffer; and

write said set to the allocation register.

24. The apparatus of claim 23, further comprising:

a line indication module to

generate a vector including a plurality of data elements, each data .element being associated with a corresponding one of the plurality of sets,

change a value of a data element in the vector to a value corresponding to a full set in response to writing the set associated with said data, element in the vector to the allocation memory, and

change the value of said data element in the vector from the allocation register to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

25. The apparatus of claim 24, wherein the line indication module is further operative to:

identify a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

26. The apparatus of claim 18, wherein the allocation memory comprises an SRAM.

27. An apparatus comprising:

an allocation memory including a plurality of allocation data elements arranged in a first plurality of sets, a plurality of said allocation data elements being associated with a corresponding plurality of buffers in a buffer memory;

a reclaim memory including a plurality of reclaim data elements arranged in a second plurality of sets, each of said reclaim data elements corresponding to an associated allocation data element and the buffer associated with said allocation data element; and

a reclaim module to

search the plurality of reclaim data elements,

identify one or more reclaim data elements to reclaim,

set the value of said one or more reclaim data elements to a value corresponding to an available buffer,

in a subsequent search, compare the allocation data elements to the associated reclaim data elements, and

change the value of an allocation data element with a value corresponding to an allocated buffer to the value corresponding to an available buffer in response to the associated reclaim data element having the value corresponding to an available buffer.

28. The apparatus of claim 27, further comprising:

a buffer manager operative to allocate the buffer associated with said allocation data element.

29. The apparatus of claim 27, wherein each of the plurality of allocation data elements comprises a single bit, and

wherein each of the plurality of reclaim data elements comprises a single bit.

30. The apparatus of claim 27, wherein the allocation memory comprises an SRAM, and

wherein the reclaim memory comprises an SRAM.

31. The apparatus of claim 27, wherein the first plurality of sets comprises a plurality of lines in the allocation memory, and

wherein the second plurality of sets comprises a plurality of lines in the reclaim memory.

32. The apparatus of claim 27, wherein, in response to receiving a trigger signal, the reclaim module is operative to:

identify each allocation data element having the value corresponding to an allocated buffer; and

set the value of each reclaim data element associated with said each allocation data element to the value corresponding to an allocated buffer.

33. The apparatus of claim 27, further comprising:

an allocation register to store one of said plurality of sets; and

a buffer manager to allocate buffers based on the values of allocation data elements in the allocation register.

34. The apparatus of claim 33, further comprising:

an allocation clear register; and

a reclaim clear register, and

wherein the buffer manager is operative to

in response to a request to clear a buffer, identify an allocation data element associated with the buffer, and

in response to identifying said allocation data element in the allocation register, setting a value of said allocation element to the value corresponding to an available buffer, and

in response to not identifying said location data element in the allocation register, writing the set including the allocation data element to the allocation clear register and setting a value of said allocation element to the value corresponding to an available buffer, and

writing the set including the reclaim data element,

associated with said allocation data element to the reclaim clear register and setting a value of said reclaim element to the value corresponding to an available buffer.

35. The apparatus of claim 33, wherein the buffer manager is operative to

monitor the values of the allocation data elements in the allocation register; and

in response to each of the allocation data elements in the allocation register having the value associated with an allocated buffer, write the values of the set of allocation data elements to the allocation memory and to the reclaim memory.

36. The apparatus of claim 33, wherein the buffer manager is operative to identify the one or more reclaim data elements to reclaim based on an aging time period.

37. An apparatus comprising:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

an allocation register; and

a buffer manager including

means for writing one of said plurality of sets into the allocation register, and

means for, in response to an allocation request,

identifying a data element in the allocation register having a value corresponding to an, available buffer,

changing the value of said data element to a value corresponding to an allocated buffer, and

allocating the buffer associated with said data element.

38. The apparatus of claim 37, wherein each of the
plurality of data elements comprises a single bit.

39. The apparatus of claim 37, wherein each of the plurality of sets comprises a line in the allocation memory.

40. The apparatus of claim 37, wherein the buffer manager further comprises:

means for, in response to a clear request for one of the plurality of buffers,

identifying a data element associated with said buffer in one of the allocation memory and the allocation register, and

changing a value of said data element to the value corresponding to an available buffer.

41. The apparatus of claim 40, wherein the buffer manager further comprises:

means for writing the set including said data element to a clear register in response to identifying the data element associated with said buffer in the allocation memory; and

means for writing the set in the clear register to the allocation memory after changing the value of said data element in the clear register.

42. The apparatus of claim 37, wherein the buffer manager further comprises:

43. The apparatus of claim 42, further comprising:

means for generating a vector including a plurality of data elements, each data element being associated with a corresponding one of the plurality of sets;

means for changing a value of a data element in the vector to a value corresponding to a full set in response to writing the set associated with said data element in the vector to the

allocation memory; and

means for changing the value of said data element in the vector from the allocation register to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

44. The apparatus of claim 43,, further comprising:

means for identifying a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

45. The apparatus of claim 37, wherein the allocation memory comprises an SRAM.

46. An apparatus comprising:

an allocation memory including a plurality of allocation data elements arranged in a first plurality of sets, a plurality of said allocation data elements being associated with a corresponding plurality of buffers in a , buffer memory;

a reclaim memory including a plurality of reclaim data elements arranged in a second plurality of sets, each of said reclaim data elements corresponding to an associated allocation data element and the buffer associated with said allocation data element; and

a reclaim module including

means for searching the plurality of reclaim data elements,

means for identifying one or more reclaim data elements to reclaim,

means for setting the value of said one or more reclaim data elements to a value corresponding to an available buffer,

means for, in a subsequent search,

comparing the allocation data elements to the associated reclaim data elements, and

means for changing the value of an allocation data element with a value corresponding to an allocated buffer to the value corresponding to an available buffer in response to the associated reclaim data element having the value corresponding to an available buffer.

47. The apparatus of claim 46, further comprising:

means for allocating the buffer associated with said allocation data element.

48. The apparatus of claim 46, wherein each of the plurality of allocation data elements comprises a single bit, and

wherein each of the plurality of reclaim data elements comprises a single bit.

49. (Withdrawn) The apparatus of claim 46, wherein the allocation memory comprises an SRAM, and

wherein the reclaim memory comprises an SRAM.

50. (Withdrawn) The apparatus of claim 46, wherein the first plurality of sets comprises a plurality of lines in the allocation memory, and

wherein the second plurality of sets comprises a plurality of lines in the reclaim memory.

51. The apparatus of claim 46, wherein the reclaim module further comprises:

means for, in response to receiving a trigger signal,

identifying each allocation data element having , the value corresponding to an allocated buffer, and

setting the value of each reclaim data element associated with said each allocation data element to the value corresponding to an allocated buffer.

52. The apparatus of claim 46, further comprising:

an allocation register to store one of said plurality of sets; and

means for allocating buffers based on the values of allocation data elements in the allocation register.

53. The apparatus of claim 52, further comprising:

an allocation clear register; and

a reclaim clear register;

means for, in response to a request to clear a buffer, identifying an allocation data element associated with the buffer;

means for, in response to identifying said allocation data element in the allocation register, setting a value of said allocation element to the value corresponding to an available buffer; and

means for, in response to not identifying said allocation data element in the allocation register,

writing the set including the allocation data, element to the allocation clear register and setting a value of said allocation element to the value corresponding to an available buffer, and

writing the set including the reclaim data element associated with said allocation data element to the reclaim clear register and setting a value of said reclaim element to the value corresponding to an available buffer.

54. The apparatus of claim 52, further comprising:

means for monitoring the values of the allocation data elements in the allocation register; and

means for, in response to each of the allocation data elements in the allocation register having the value associated with an allocated buffer, writing the values of the set of allocation data elements to the allocation memory and to the reclaim memory.

55. The apparatus of claim 46, further comprising:

means for identifying the one or more reclaim data elements to reclaim based on an aging time period.

56. A system comprising:

a switching module to receive and switch packets;

a buffer memory including a plurality of buffers to store received packets; and

a buffer management module including:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding one of the plurality of buffers in the buffer memory;

an allocation register; and

a buffer manager to

write one of said plurality of sets into the allocation register, and

in response to an allocation request,

identify a data element in the allocation register having a value corresponding to an available buffer,

change the value of said data element to a value corresponding to an allocated buffer, and

allocate the buffer associated with said data element.

57. The system of claim 56, wherein each of the plurality of data elements comprises a single bit.

58. The system of claim 56, wherein each of the plurality of sets comprises a line in the allocation memory.

59. The system of claim 56, wherein the buffer manager is further operative to:

in response to a clear request for one of the plurality of buffers,

identify a data element associated with said buffer in one of the allocation memory and the allocation register; and

change a value of said data element to the value corresponding to an available buffer.

60. The system of claim 59, wherein the buffer manager is further operative to:

in response to identifying the data element associated with said buffer in the allocation memory,

write the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

write the set in the clear register to the allocation memory.

61. The system of claim 56, wherein the buffer manager is further operative to:

monitor the values of each of the data elements in the allocation register; and

in response to each of said data elements having the value corresponding to an allocated buffer,

write the data elements in the allocation register back to the allocation memory;

identify a set including at least one data element having the value corresponding to an available buffer; and

write said set to the allocation register.

62. The system of claim 61, further comprising:

a line indication module to

generate a vector including a plurality of data elements, each data element being associated with a corresponding one of the plurality of sets,

change a value of a data element in the vector to a value corresponding to a full set in response to writing the set associated with said data element in the vector to the allocation memory, and

change the value of said data element in the vector from the allocation register to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

63. The system of claim 62, wherein the line indication module is further operative to:

identify a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

64. The system of claim 56, wherein the allocation memory comprises, an SRAM.

65. A system comprising:

a switching module to receive and switch packets;

a buffer memory including a plurality of buffers to store receive5 packets; and

a buffer management module including:

an allocation memory including a plurality of allocation data elements arranged in a first plurality of sets, a plurality of said allocation data elements being associated with a corresponding plurality of buffers in the buffer memory;

a reclaim memory including a plurality of reclaim data elements arranged in la second' plurality of sets, each of said reclaim data elements corresponding to an associated allocation data element and the buffer associated with said allocation data

element; and

a reclaim module to

search the plurality of reclaim data elements,

identify one or more reclaim data elements to reclaim,

set the value of said one or more reclaim data elements to a value corresponding to an available buffer,

in a subsequent search, compare the allocation data elements to the associated reclaim data elements, and

change the value of an allocation data element with a value corresponding to an allocated buffer to the value corresponding to an available buffer in response to the associated reclaim data element having the value corresponding to an available buffer.

66. The system of claim 65, further comprising:

a buffer manager operative to allocate the buffer associated with said allocation data element.

67. The system of claim 65, wherein each of the plurality of allocation data elements comprises a single bit, and

wherein each of the plurality of reclaim data elements comprises a single bit.

68. The system of claim 65, wherein the allocation memory comprises an SRAM, and wherein the reclaim memory comprises an SRAM.

69. The system of claim 65, ,wherein the first plurality of sets comprises a plurality of lines in the allocation memory, and

wherein the second plurality of sets comprises a plurality of' lines in the reclaim memory.

70. The system of claim 65, wherein, in response to receiving a trigger signal, the reclaim module is operative to:

identify each allocation data element having the value corresponding to an allocated buffer; and

set the value of each reclaim data element associated with said each allocation data element to the value

corresponding to an allocated buffer.

71. The system of claim 65, further comprising:

an allocation register to store one of said plurality of sets; and

a buffer manager to allocate buffers based on the values of allocation data elements in the allocation register.

72. The system of claim 71, further comprising:

an allocation clear register; and a reclaim clear register; and

a reclaim clear register, and

wherein the buffer manager is operative to

in response to a request to clear a buffer, identify an allocation data element associated with the buffer, and

in response to identifying said allocation data element in the allocation register, setting a value of said allocation element to the value corresponding to an available buffer, and

in response to not identifying said allocation data element in the allocation register, writing the set including the allocation data element to the allocation clear register and setting a value of said allocation element to the value corresponding to an available buffer,

writing the set including the reclaim data element associated with said allocation data element to the reclaim clear register and setting a value of said reclaim element to the value corresponding to an available buffer.

73. The system of claim 71, wherein the buffer manager is operative to

monitor the values of the allocation data elements in the allocation register; and

in response to each of the allocation data elements in the allocation register having the value associated with an allocated buffer, write the values of the set of allocation data elements to the allocation memory and to the reclaim memory.

74. The system of claim 71, wherein the buffer manager is operative to identify the

one or more reclaim data elements to reclaim based on an aging time period.

75. A system comprising:

a switching module including means for receiving and switching packets;

a buffer memory including a plurality of buffers for storing received packets; and

a buffer management module including:

an allocation memory including a plurality of data elements arranged in a plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

an allocation register; and

a buffer manager including

means for writing one of said plurality of sets into the allocation register, and

means for, in response to an allocation request,

identifying a data element in the allocation register having a value corresponding to an available buffer,

changing the value of said data element to a value corresponding to an allocated buffer, and

allocating the buffer associated with said data element.

76. The system of claim 75, wherein each of the plurality of data elements comprises a single bit.

77. The system of claim 75, wherein each of the plurality of sets comprises a line in the allocation memory.

78. The system of claim 75, wherein the buffer manager further comprises:

means for, in response to a clear request for one of the plurality of buffers,

identifying a data element associated with said buffer in one of the allocation memory and the allocation register, and

changing a value of said data element to the value corresponding to an available buffer.

79. The system of claim 78, wherein the buffer manager further comprises:

means for writing the set including said data element to a clear register in response to identifying the data element associated with said buffer in the allocation memory; and

means for writing the set in the clear register to the allocation memory after changing the value of said data element in the clear register.

80. The system of claim 75, wherein the buffer manager further comprises:

means for monitoring the values of each of the data elements in the allocation register; and

means for, in response to each of said data elements having the value corresponding to an allocated buffer,

writing the data elements in the allocation register back to the allocation memory,

identifying a set including at least one data element having the value corresponding to an available buffer, and

writing said set to the allocation register.

81. The system of claim 80, further comprising:

means for generating a vector including a plurality of data elements, each data element being associated with a corresponding one of the plurality of sets;

means for changing a value of a data element in the vector to a value corresponding to a full set in response to writing the set associated with said data element in the vector to the allocation memory; and

means for changing the value of said data element in the vector from the allocation register to a value corresponding to an available set in response to the value of ,one of the data elements in said set being changed to the value corresponding to an available buffer.

82. The system of claim 81, further comprising:

means for identifying a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

83. The system of claim 75, wherein the allocation memory comprises an SRAM.

84. A system comprising:

a switching module including means for receiving and switching packets;

a buffer memory including a plurality of buffers for storing received packets; and

a buffer management module including:

an allocation memory including a plurality of allocation data elements arranged in a first plurality of sets, a plurality of said allocation data elements being associated with a corresponding plurality of buffers in a buffer memory;

a reclaim memory including a plurality of reclaim data elements arranged in a second plurality of sets, each of said reclaim data elements corresponding to an associated allocation data element and the buffer associated with said allocation data element; and

a reclaim module including

means for searching the plurality of reclaim data elements,

means for identifying one or more reclaim data elements to reclaim,

means for setting the value of said one or more reclaim data elements to a value corresponding to an available buffer,

means for, in a subsequent search,

comparing the allocation data elements to the associated reclaim data elements, and

means for changing the value of an allocation data element with a value corresponding to an allocated buffer to the value corresponding to an available buffer in response to the associated reclaim data element having the value corresponding to an available buffer.

85. The system of claim 84, further comprising:

means for allocating the buffer associated with said allocation data element.

86. The system of claim 84, wherein each of the plurality of allocation data elements comprises a single bit, and

wherein each of the plurality of reclaim data elements comprises a single bit.

87. The system of claim 84, wherein the allocation memory comprises an SRAM, and

wherein the reclaim memory comprises an SRAM.

88. The system of claim 84, wherein the first plurality of sets comprises a plurality of lines in the allocation memory, and

wherein the second plurality of sets .comprises a plurality of 'lines in the reclaim memory.

89. The system of claim 84, wherein the reclaim module further comprises:

means for, in response to receiving a trigger signal,

identifying each allocation data element having the value corresponding to an allocated buffer, and setting the value of each reclaim data element associated with said each allocation data element to the value corresponding to an allocated buffer.

90. The system of claim 84, further comprising:

an allocation. register to store one of said plurality of sets; and

means for allocating buffers based on the values of allocation data elements in the allocation register.

91. The system of claim 90, further comprising:

an allocation clear register; and

a reclaim clear register;

means for, in response to a request to clear a buffer, identifying an allocation data element associated with the buffer;

means for, in response to identifying said allocation data element in the allocation register, setting a value of said allocation element to the value corresponding to an available buffer; and

means for, in response to not identifying said allocation data element in the allocation register,

writing the set including the allocation data element to the allocation clear register and

setting a value of said allocation element to the value

corresponding to an available buffer, and

writing the set including the reclaim data element associated with said allocation data element to the reclaim clear register and setting a value of said reclaim element to the value corresponding to an available buffer.

92. The system of claim 90, further comprising:

means for monitoring the values of the allocation data elements in the allocation register; and

means for, in response to each of the allocation data elements in the allocation register having the value associated with an allocated buffer, writing the values of the set of allocation data elements to the allocation memory and to the reclaim memory.

93. The system of claim 90, further comprising:

means for identifying the one or more reclaim data elements to reclaim based on an aging time period.

94. A computer-readable medium having instructions stored thereon, which, when executed by a processor, causes the processor to perform operations comprising:

writing one of a plurality of sets in an allocation memory into an allocation register, wherein the allocation memory includes a plurality of data elements arranged in the plurality of sets, each of said data elements being associated with a corresponding plurality of buffers in a buffer memory;

in response to an allocation request,

identifying a data element in the allocation register having a value corresponding to an available buffer;

changing the value of said data element to a value corresponding to an allocated buffer; and

allocating the buffer associated with said data element.

95. The computer-readable medium of claim 94, wherein each of the plurality of data

elements comprises a single bit.

96. The computer-readable medium of claim 94, wherein each of the plurality of sets comprises a line in the allocation memory.

97. The computer-readable medium of claim 94, further comprising:

in response to a clear request for one of the plurality of buffers,

identifying a data element associated with said buffer in one of the allocation memory and the allocation register; and

changing a value of said data element to the value corresponding to an available buffer.

98. The computer-readable medium of claim 97, further comprising:

in response to identifying the data element associated with said buffer in the allocation memory,

writing the set including said data element to a clear register; and

after changing the value of said data element in the clear register,

writing the set in the clear register to the allocation memory.

99. The computer-readable medium of claim 94, further comprising:

monitoring the values of each of the data elements in the allocation register; and

in response to each of said data elements having the value corresponding to an allocated buffer,

writing the data elements in the allocation register back to the allocation memory;

identifying a set including at least one data element having the value corresponding to an available buffer; and

writing said set to the allocation register.

100. The computer-readable medium of claim 99, .further comprising:

providing a vector including a plurality of data elements, each data element being associated with a corresponding one of the plurality of sets;

changing a value of a data element in the vector from the allocation register to a value corresponding to a full set in response to writing the set associated with said data element in the

vector to the allocation memory; and

changing the value of said data element in the vector to a value corresponding to an available set in response to the value of one of the data elements in said set being changed to the value corresponding to an available buffer.

101. The computer-readable medium of claim 100, further comprising:

identifying a set including at least one data element with the value corresponding to an available buffer by examining the values of the data elements in the vector.

102. A computer program comprising:

searching an allocation memory including a plurality of allocation data elements arranged in a second plurality of sets, each of said allocation data elements corresponding to an associated reclaim data element and the buffer associated with said reclaim data element;

searching a reclaim memory including a plurality of reclaim data elements arranged in a first plurality of sets, a plurality of said reclaim data elements being associated with a corresponding plurality of buffers in a buffer memory;

identifying one or more reclaim data elements to reclaim;

setting the value of said one or more reclaim data elements to a value corresponding to an available buffer; and

in a subsequent search, searching an allocation memory including a plurality of allocation data elements arranged in a second plurality of sets, each of said allocation data elements corresponding to an associated reclaim data element and the buffer associated with said reclaim data element;

comparing the allocation data elements to the associated reclaim data elements; and

changing the value of an allocation data element with a value corresponding to an allocated buffer to the value corresponding to an available buffer in response to the associated reclaim data element having the value corresponding to an available buffer.

103. The computer program of claim 102, further comprising:

allocating the buffer associated with said allocation data element.

104. The computer program of claim 102, wherein each of the plurality of allocation data elements comprises a single bit., and

wherein each of the plurality of reclaim data elements comprises a single bit.

105. The computer program of claim 102, wherein the first plurality of sets comprises a plurality of lines in the allocation memory, and

wherein the second plurality of sets comprises a plurality of lines in the reclaim memory.

106. The computer program of claim 102, further comprising:

in response to receiving a trigger signal,

identifying each allocation data element having the value corresponding to an allocated buffer; and

setting the value of each reclaim data element associated with said each allocation data element to the value corresponding to an allocated buffer.

107. The computer program of claim 102, further comprising:

reading one of said plurality of sets into an allocation register; and

allocating buffers based on the values of allocation data elements in the allocation register.

108. The computer program of claim 107, further comprising:

in response to a request to clear a buffer,

identifying an allocation data element associated with the buffer; and

in response to identifying said allocation data element in the allocation register, setting a value of said allocation element to the value corresponding to an available buffer; and

in response to not identifying said allocation data element in the allocation register,

writing the set including the allocation data element to an allocation clear register and setting a value of said allocation element to the value corresponding to an available buffer; and

writing the set including the reclaim data element associated with said allocation data element to a reclaim clear register and setting a value of said reclaim element to the value corresponding to an available buffer.

109. The computer program of claim 102, further comprising:

monitoring the values of the allocation data elements in the allocation register; and

in response to each of the allocation data elements in the allocation register having the value associated with an allocated buffer, writing the values of the set of allocation data elements to the allocation memory and to the reclaim memory.

110. The computer program of claim 102, wherein said identifying comprises identifying the one or more reclaim data elements to reclaim based on an aging time period.

111. The method of claim 1, wherein each of the plurality of sets is a non-empty set.

Evidence Appendix

None.

Related Proceedings Appendix

None.